DESIGN OF HIGH FREQUENCY CMOS FRACTIONAL-N FREQUENCY DIVIDER

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Abstract – This paper discussed the circuit level design and simulation of fractional-N frequency divider, a circuit block used mainly in frequency synthesizer. The design was done in schematic level. A low power 0.5 micron CMOS technology called CMOSIS5 used for modeling the circuit devices. The frequency divider was design for 900 MHz GSM standard mobile communication application. For the simulation, circuit level simulator SPICE was used. The circuit was run under 1 GHz input frequency. Simulation results show that the circuit was running well in this frequency input.

Keywords: Frequency Divider, Multiple modulus, PLL Synthesizer.

1. INTRODUCTION

A frequency divider is one of the important blocks for the phase-locked loop (PLL) synthesizer, which is widely used in many applications such as radar, digital communication, and electronic imaging. “Frequency synthesis” was used for the first time in 1943 by Finden when he described the generation of frequencies that are multiples of a reference frequency [1]. A PLL synthesizer consists of a phase detector (PD), a loop filter (LF), a voltage controlled oscillator (VCO), and a frequency divider (FD). The block diagram of a PLL synthesizer and its linear model is shown in Fig. 1. The frequency of the PLL synthesizer input (reference signal, \( f_r \)) is a fixed value and the frequency of its output signal (\( f_o \)) is the reference frequency multiplied by \( N \). The frequency of the output signal can be varied by changing the division ratio (N) of the frequency divider. PLL synthesizers exhibit excellent phase noise performance over a wide tuning range and are easier to implement in monolithic form compared to the others frequency synthesizers [2].

For many applications, for example in radio frequency systems, need a frequency synthesizer that is able to change in small and precise steps at high speed. To have a small step, the reference frequency should be set to a very low frequency compared to the output frequency. This condition makes the division ratio \( N \) very large and the loop bandwidth (natural frequency) very small, thus the settling time will be very slow. Another problem with a low reference frequency is the wide variation of \( N \). Since the damping factor and natural frequency are functions of the division ratio \( N \), the large change in \( N \) will have an impact on stability, settling time, and phase error. To solve this problem the division ratio \( N \) is made a fractional number (fractional-N PLL synthesizer) [3]. The discussions about the linear and non-linear modeling of the PLL synthesizer have been done in Mujiono paper [4]. The impact of the multiple modulus, for fractional-N frequency divider implementation, to the output signal was also discussed in the same paper. There are many approach of fractional-N frequency divider implementation. Basically, it can be categorized in two approaches: conventional and non-conventional. The discussion of implementation of fractional-N frequency divider using Programmable Devices (FPGA) has been done in Mujiono paper [5].

In this paper we presented the possible implementation of fractional-N frequency divider for monolithic circuit. The most popular technology for the digital system is metal oxide semiconductor (MOS) technology due to the high density and low power of the complementary MOS (CMOS) fabrication processes. Some research in monolithic PLL synthesizers using CMOS technology has been reported in recent years. A fully monolithic PLL synthesizer without any external blocks was implemented in 0.45 micron CMOS technology [6].

2. FRACTIONAL FREQUENCY DIVIDER

A frequency divider divides the frequency of the input signal by \( N \) to get the output frequency at \( 1/N \) times the input frequency. In the PLL frequency synthesizer application, the value of the divider is not fixed but variable with the range from a minimum value (\( N_{\text{min}} \)) to a maximum value (\( N_{\text{max}} \)) with a certain step size as illustrated in Fig. 2. The mean of the divider value is:

\[
N_{\text{mean}} = \left( N_{\text{min}}N_{\text{max}} \right)^{1/2}
\]
Division by a fractional number is possible using multiple modulus divider, for example dual modulus: N and N+1. By periodically alternating the division ratio between N and N+1, the result, on average, is a fraction between N and N+1. For example, if the counter divides by 181 for 57 cycles (out of 100 cycles) and divides by 182 in the remaining 43 cycles, the counter will be working as it was a 181.43 divider.

The value N is the integer part of the division ratio. The control signal responsible for selecting the division ratio (either N or N+1) comes from the overflow (Co) signal of the full-adder (FA) output. The full-adder here is a synchronous adder, and the clock signal comes from the output of the divider. The output of the full adder is sent back to the input for the next addition. Another input comes from the fractional part of the division ratio F (see Fig. 3). For a division ratio of 181.70, the integer part (N) is 181 while the fractional part (F) is 0.70.

The divider consists of two asynchronous counters (counter_1 and counter_2), a prescaler V/V+1, a delay circuit, and an adder. Both counter_1 and counter_2 are up counters with counter_2 value (N2) always less than counter_1 value (N1). The prescaler is a dual modulus synchronous counter whose value is controlled by the presc_ctrl signal generated by counter_2. For example if the presc_ctrl signal is "high", the prescaler works as a V+1 counter and if presc_ctrl signal is "low", the prescaler works as a V counter. The delay circuit is used to delay the presc_ctrl signal by one clock cycle (to get a ratio of N+1) when the adder circuit sends the overflow signal. The adder circuit is used to generate the control signal for the divider modulus, N or N+1.

In this paper, the input signal to the fractional-N divider is assumed to have variation between the frequency of 880 MHz and 920 MHz with resolution 200 KHz, and the output signal is assumed to have frequency of 5 MHz. Thus, the fractions of division are 0.04, 0.08, 0.12, 0.16, ..., 0.92, and 0.96. For these values the overflow signal always repeat every 25 cycles of the input. The number of times it goes high within these cycles depends on the specific fraction. For a fraction of 0.04, it goes high for one cycle every 25 cycles, hence its frequency is 200 KHz since clock (f’out) is 5 MHz. This case will be the same if the fraction is 0.96. For the other fractions, the frequency will be the same or higher. This overflow signal causes spurious noise at the VCO input[4]. As the spurious signal rejection is lower for higher frequencies of the overflow signal, a worst case value of 200 KHz is used for the overflow frequency when spurious rejection is considered.

These values, division ratio variations, are used for GSM standard mobile communication application. Thus the fractional-N divider has a division ratio range between 176 and 184 with a 0.04 step. For this division ratio range, in this research, N1 is set to fixed number 44, V is set to 4, and N2 (depends on the combination of d1, d2, d3, and d4) is made variable between 0 and 15, but only 9 (0 to 8) of them are needed.

3. CIRCUIT LEVEL IMPLEMENTATION

System level design of the fractional-N frequency divider has been discussed in part 2. The circuit level description of the fractional-N frequency divider will be discussed in part 3. A 3.3 volt MOSIS complementary metal oxide semiconductor (CMOS) technology from MOSIS, CMOSIS5, which supports low voltage operation, has been used to design the fractional-N frequency divider.
The frequency divider circuit is mainly implemented using a dynamic single-phase clock called a true single-phase clock (TSPC) circuit technique that is suitable for high-speed applications [7]. Other parts of the circuit are designed in standard CMOS complementary logic circuits and an And-Or-Invert (AOI) logic function. The important issue in high-speed digital circuit design is transistor sizing since the size of each device controls both its capacitance and current capability, where both of them are will be controlled the circuit speed.

The circuit designed for the dual-modulus divider is shown in Fig. 5. Here, counter_1 and counter_2 have been merged into only one 6-bit asynchronous counter. The input signal (from the VCO) comes to the in_signal and the scaled down signal output port is Divider_out. Initially, the content of the counter is 0 and the prescaler is dividing by 5. When the counter reaches \( N_2 \), which is determined by input d1, d2, d3, and d4, the res output of the RS-FF becomes "high". This causes the presc_ctrl to go "low" and prescaler starts dividing by 4.

The counter continues counting up until its contents reach 44, at which point the output of the 3-input NAND gate NAND3 (res2) goes "low" and makes the clear signal "high", which causes the counter and RS-FF to be reset. However, the presc ctrl state is not changed until next the clock cycle when the output of the DFF-X goes "high". This guarantees synchronization with the clock pulse. The circuit operation explained above happens if the Overflow signal is "low". If the Overflow signal is "high", then when the counter reaches the final count and the output of the RS-FF is "low", two cycles will be needed (as opposed to one in the previous case) to change the presc ctrl signal. Thus, the prescaler control is delayed by an additional clock cycle. It needs 353 transistor to implement the fractional-N frequency divider.

### 3.1. Prescaler

One of the important parts in the fractional-N divider explained above is the prescaler circuit. The prescaler circuit operates at high frequency (about 900 MHz) and the remaining logic circuits operate at most at 225 MHz. There are two types of prescaler: fixed rate and dual modulus. In this research, the dual modulus type is used since two values, \( V \) and \( V+1 \) (4 and 5), are needed. The prescaler circuit consists of three positive transition D latches arranged in a master-slave configuration with negative feedback [8]. The output signal from the prescaler (clk_out) is equal to the input frequency divided by 4 or 5 depending on the prescaler control (presc_ctrl). If the prescaler control is "high" the output is divided by 5 and if the prescaler control is "low" then the output is divided by 4.

### 3.2. Full-Adder

As has already been explained in Part II, the fractional part of the divider value is in the range between 0.04 to 0.96 with a step of 0.04. To have good resolution much more than 16 bits are needed to implement these values in a fractional binary system. In this research these fractional values were multiplied by 100, thus now the values are in the range between 4 and 96 with step 4. Therefore the overflow signal is asserted if the result of the addition is 100 or more. A decimal number from 4 to 96 input needs 8-bit data binary. This 8-bit input binary number is the d0-d7 inputs. A small modification is needed for the result of 100 or above. If the result is below 100, this number can be directly added to the original value. But if the result is 100 or above, this value needs to be added with 28 before being added to the original value. Two 8-bit full-adder, control, multiplexer, and accumulator blocks perform this function. Since the addition operation performed in this block does not have a high speed requirement (only 5 MHz), the circuit realization is built using standard CMOS (CMOS complementary) techniques.
4. CIRCUIT SIMULATION

The circuit has been run several times for simulation. The standard circuit level simulator called SPICE has been employed for that purpose. The 0.5 micron CMOS technology from MOSIS, called CMOSIS5, has been used for the transistor model. Some of the simulation will be presented here. The 1 GHz signal has been used for the fractional-N divider input.

Fig. 6 shows the output waveforms of the asynchronous counter. The input signal of the counter is the output signal from the prescaler (presc_out), and the output signal is the inverse of the last D-latch output, Q5b. Q0b, Q1b, Q2b, Q3b, and Q4b signals are the output of the D-latches used to build the counter. When the clear signal is asserted, the prescaler control (presc_ctrl) goes "high", and the prescaler acts as a divide by 5. After the counter reaches N2 (7) the prescaler control goes "low" and now the prescaler acts as a divide by 4 until the counter reaches N1 (44). It can be seen that the signal period of the prescaler output is wider when the prescaler control (presc_ctrl) is "high" compared to when the prescaler control is "low". There are 44 presc_out signals in total between the clear signal and the next clear signal. The output of the counter is Q5b.

The next simulation is for the fractional-N frequency divider. Simulation of fractional-N divider needs quite a lot of memory space and simulation time. For an example, with the division ratio set to 183.92 in every 100 cycles of the output signal, 92 cycles are the result of division by 184 and the other 8 cycles are the result of division by 183. Thus at least 25 cycles of the output signals are needed to see one whole cycle of fractional division.

Fig. 7 shows the waveforms of the divider output when the division ratio is set to 183.60. This division ratio is obtained by setting the scale factor of the integer (N2) to 7 (0111) and fractional input to 60 (0111100) of the fractional divider circuit. As explained in Chapter 4, Ni is fixed at 44. The waveforms consist of divider input signal (f_in), prescaler control (presc_ctrl), clear (clear), overflow (Overflow), and divider output signal (Divider_out). The frequency of the input signal is set to 1 GHz.
Just after the first clear signal appears (at time 188.1 ns), the Divider_out signal goes “high” and the contents of the accumulator becomes 60 and the Overflow signal is “low”, the counter will count until 183 before the second clear signal is generated. The second Divider_output signal changes the contents of the accumulator to 20 and Adder circuit sends the overflow signal; now the counter will count until 184. Thus, for 5 cycles period of the output signal, the input frequency will be divided by 183 for two cycles (cycle 1 and cycle 3) and divided by 184 for the other 3 cycles. The difference between a divide by 183 and divide by 184 cannot be seen from the divider output (Divider_out) waveform shown here, since the difference is very small.

A time period of 10 cycles of the Divider_out signal measured from the simulation starting at the first clear signal is shown in Table 1 below.

Table 1: Time periods of the frequency divider output measured from simulation

<table>
<thead>
<tr>
<th>Cycle #</th>
<th>T(μS)</th>
<th>Cycle #</th>
<th>T(μS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>183.0</td>
<td>6</td>
<td>183.0</td>
</tr>
<tr>
<td>2</td>
<td>184.0</td>
<td>7</td>
<td>184.0</td>
</tr>
<tr>
<td>3</td>
<td>183.0</td>
<td>8</td>
<td>183.0</td>
</tr>
<tr>
<td>4</td>
<td>184.0</td>
<td>9</td>
<td>184.0</td>
</tr>
<tr>
<td>5</td>
<td>183.9</td>
<td>10</td>
<td>184.0</td>
</tr>
</tbody>
</table>

The total period for the 10 cycles of simulation is 1.8359×10⁻⁶ second. The average time period for each cycle is 1.8359×10⁻⁷ second. This number is slightly different from the time period resulting from the calculation, i.e., 183.6/(1×10⁵) = 1.836×10⁻⁷ second. This difference can be reduced if more cycles are included in the measurement.

5. SUMMARY AND CONCLUSION

In this paper, the fractional-N frequency divider has been designed and simulated at the schematic level. The fractional-N divider designed for a division ratio range between 176 and 184 with a 0.04 step. The circuit was designed for input frequency about 900 MHz. The circuit realization was performed at the schematic level using the low power CMOSIS5 0.5 micron technology. About 353 transistor was needed to implement the frequency divider. The simulation was performed using SPICE, a standard circuit level simulation tool. The simulation results shown that the divider circuit was working well at the 1 GHz.

REFERENCES


Totok Mujiono finished his S1 degree in Electrical Engineering from Institute of Technology Sepuluh Nopember (ITS) in 1988 and S2 degree in Computer Science from University of Indonesia (UI) in 1990. His main research is high-level modeling and implementation of frequency-synthesizer, including: behavioral modeling of phase-locked loop (PLL) and FPGA based implementation of digital PLL and direct discrete synthesizer (DDS).